Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims:

1. (original) A semiconductor die package comprising;
a semiconductor die;
a leadframe having a chemically-etched surface; and
a capsule enclosing said die and at least a portion said leadframe.

2. (original) The semiconductor package of Claim 1 wherein said leadframe consists essentially of copper alloy.

3-6. (canceled)

7. (previously presented) A semiconductor package comprising:
a semiconductor die;
a leadframe having a chemically-etched surface; and
a capsule enclosing said die and at least a portion said leadframe;
said package further comprising an organo-metallic coating on the surface of the leadframe.

8-20. (canceled)

21. (previously presented) The semiconductor package of Claim 1 wherein the arithmetic mean deviation of a profile of said chemically-etched surface is in the range of 0.050 µm to 0.170 µm.

22. (previously presented) The semiconductor package of Claim 21 wherein the mean peak-to-valley height of said chemically-etched surface is in the range of 0.180 µm to 0.700 µm.

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23. (previously presented) The semiconductor package of Claim 22 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 µm to 1.500 µm.

24. (previously presented) The semiconductor package of Claim 21 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 µm to 1.500 µm.

25. (previously presented) The semiconductor package of Claim 24 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

27. (previously presented) The semiconductor package of Claim 22 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

27. (previously presented) The semiconductor package of Claim 21 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

28. (previously presented) The semiconductor package of Claim 1 wherein the mean peak-to-valley height of said chemically-etched surface is in the range of 0.180 µm to 0.700 µm.

29. (previously presented) The semiconductor package of Claim 28 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 µm to 1.500 µm.

30. (previously presented) The semiconductor package of Claim 29 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

31. (previously presented) The semiconductor package of Claim 28 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

32. (previously presented) The semiconductor package of Claim 1 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 µm to 1.500 µm.

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33. (previously presented) The semiconductor package of Claim 32 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

34. (previously presented) The semiconductor package of Claim 1 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 µm to 0.750 µm.

35. (previously presented) The semiconductor package of any one of Claims 21 to 34 further comprising an organo-metallic coating on the surface of the leadframe.

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